WHAT IS CLAIMED IS:

1. A data transmission device comprising:

clock generation circuit generating a clock signal;

jitter supply circuit allowing the clock signal generated by the clock generation circuit to include jitter; and

a data transmission circuit transmitting data in sync with the clock signal including the jitter.

2. The data transmission device according to claim 1, wherein

the jitter supply circuit adjusts the amount of modulation and/or the frequency of the jitter included in the clock signal.

3. The data transmission device according to claim 1, wherein

the jitter supply circuit supplies, as the jitter, at least any one of a sinusoidal jitter and a random jitter.

4. The data transmission device according to claim 2, wherein

the jitter supply circuit supplies, as the jitter, at least any one of a sinusoidal jitter and a random jitter.

5. An I/O interface circuit comprising:

clock generation circuit generating a first clock signal;

jitter supply circuit allowing the first clock

signal generated by the clock generation circuit to include jitter; and

a data transmission circuit transmitting data in sync with the first clock signal including the jitter.

6. The I/O interface circuit according to claim 5, wherein

the jitter supply circuit adjusts the amount of modulation and/or the frequency of the jitter included in the first clock signal.

7. The I/O interface circuit according to claim 5, wherein

the jitter supply circuit supplies, as the jitter, at least any one of a sinusoidal jitter and a random jitter.

8. The I/O interface circuit according to claim 6, wherein

the jitter supply circuit supplies, as the jitter, at least any one of a sinusoidal jitter and a random jitter.

9. The I/O interface circuit according to claim 5, further comprising

a data reception circuit receiving data, wherein

the clock generation circuit also supplies a second clock signal to the data reception circuit,

the data transmission circuit includes

pattern generation circuit generating a data pattern for a jitter resistance test, and

transmission circuit allowing the data pattern

generated by the pattern generation circuit to be transmitted in sync with the first clock signal, and

the data reception circuit includes

reception circuit allowing the data pattern received by the transmission circuit to be received in sync with the second clock signal, and

pattern comparison circuit comparing the data pattern received by the reception circuit with an expectation value to output a comparison result.

10. The I/O interface circuit according to claim 9, further comprising

measurement result storage circuit associatively storing the comparison result delivered by the pattern comparison circuit and information on the amount of modulation and/or the frequency of the jitter supplied by the jitter supply circuit.

11. The I/O interface circuit according to claim 9, further comprising

jitter supply circuit control circuit controlling the jitter supply circuit to vary the amount of modulation and/or the frequency of the jitter in accordance with the comparison result delivered by the pattern comparison circuit and a measurement procedure for the jitter resistance.

12. The I/O interface circuit according to claim 9, wherein

the jitter supply circuit control circuit controls the jitter supply circuit so as to vary the amount of

modulation of the jitter when the comparison result delivered by the pattern comparison circuit indicates a match whereas varying the frequency of the jitter when the comparison result delivered by the pattern comparison circuit indicates a mismatch.

13. The I/O interface circuit according to claim 9, wherein

the pattern generation circuit in the data transmission circuit further comprises a function for including data of a contiguous sequence of 0s or 1s in the data pattern, and

the pattern comparison circuit in the data reception circuit further comprising

a first function for detecting the data of a contiguous sequence of 0s or 1s having been received, and

a second function for forcing the comparison result to indicate a match when the first function detects the data of a contiguous sequence of 0s or 1s having been received.

14. The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit replaces part of the data pattern with data of a contiguous sequence of 0s or 1s, thereby allowing the data pattern to include the data of a contiguous sequence of 0s or 1s.

15. The I/O interface circuit according to claim

13, wherein

the pattern generation circuit in the data transmission circuit inserts data of a contiguous sequence of 0s or 1s into a midpoint of the data pattern, thereby allowing the data pattern to include the data of a contiguous sequence of 0s or 1s.

16. The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit further comprises a function for adjusting a cycle in a case of data of a contiguous sequence of 0s or 1s being included in the data pattern in that cycle.